In the Claims:

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of forming a silicon dioxide layer, comprising:

providing a semiconductor substrate, the semiconductor substrate ~~having~~ including at least one silicon surface region ~~having~~ with a curved surface;

roughening the surface of the at least one silicon surface region to produce a layer of porous silicon, wherein roughening the surface of the at least one silicon surface region includes forming pores, the pores each having a width of less than 20 nm and a pore depth of less than 20 nm;

thermally oxidizing the at least one roughened curved silicon surface region; and

oxidizing the at least one silicon surface region to produce an oxidized portion within the semiconductor substrate which ends at a depth, the depth being greater than the pore depth of the pores;

wherein the surface regions which are not to be oxidized are covered with a masking layer before roughening the surface of the at least one silicon surface region.

2. (Original) The method of claim 1, wherein roughening the surface of the at least one silicon surface region includes producing pores, the pores each having a size of less than 10 nm.

3. (Original) The method of claim 2, wherein roughening the surface of the at least one silicon surface region includes producing pores, the pores each having a size of less than 5 nm.

4. (Original) The method of claim 1, wherein roughening the surface of the at least

one silicon surface region includes etching the surface region.

5. (Original) The method of claim 4, wherein etching the surface region includes etching in a solution containing phosphoric acid.

6. (Original) The method of claim 4, wherein etching the surface region includes etching in a solution including H_2SO_4, HF and HNO_3.

7. (Original) The method of claim 6, wherein etching the surface region includes etching in a solution having a composition of H_2SO_4:HF:HNO_3 = 7:1:0.01.

8. (Original) The method of claim 4, wherein roughening the surface of the at least one silicon surface region includes electrochemically etching the surface region.

9. (Original) The method of claim 8, wherein roughening the surface of the at least one silicon surface region includes etching the surface region with a mixture of hydrofluoric acid and ethyl alcohol.

10. (Original) The method of claim 9, wherein roughening the surface of the at least one silicon surface region includes etching the surface region with a mixture of 49% aqueous hydrofluoric acid and pure ethyl alcohol at a ratio of 0.75:0.25.

11. (Original) The method of claim 8, wherein roughening the surface of the at least one silicon surface region includes etching the surface region with a 6% aqueous solution of hydrofluoric acid.

12. (Canceled)

13. (Currently Amended) The method of claim [[12]] 1, wherein the masking layer includes silicon nitride.

14. (Original) The method of claim 1, wherein thermally oxidizing the at least one roughened silicon surface forms a silicon dioxide layer having a thickness larger than the pore depth of the pores.

15. (Original) The method of claim 1, wherein the silicon surface region includes monocrystalline silicon.

16. (Currently Amended) A method of producing a storage trench capacitor for a memory cell ~~having~~ including an isolation collar, comprising:

providing a semiconductor substrate, the semiconductor substrate ~~having~~ including a main surface;

providing a trench in the semiconductor substrate, the trench extending from the main surface into the semiconductor substrate, the trench ~~having~~ including an upper and a lower portion, the trench ~~having~~ including a curved inner surface of silicon;

masking the silicon surface region of the upper portion of the trench which is not to be oxidized with a masking layer;

~~and~~ exposing the silicon surface region of the lower portion of the trench on which a silicon dioxide layer is to be formed;

roughening the ~~surface of the curved~~ exposed silicon surface region in the lower portion of the trench to produce a layer of porous silicon, the masking layer having a material which prevents roughening of an underlying material during roughening of the ~~curved~~ exposed silicon surface region;

thermally oxidizing the roughened ~~curved~~ silicon surface region;

extending the trench into the semiconductor substrate to form a bottom portion of the trench beneath the lower portion of the trench;

forming a first electrode of the capacitor in the semiconductor substrate adjacent to the bottom portion of the trench;

forming a dielectric layer of the capacitor in the bottom portion of the trench; and

forming a second electrode of the capacitor in the bottom portion of the trench.

17. (Original) The method of claim 16, wherein the masking layer includes silicon nitride.

18. (Currently Amended) The method of claim 16, wherein roughening the ~~surface of the curved~~ exposed silicon surface region includes etching the exposed silicon surface region.

19. (Currently Amended) The method of claim16, wherein roughening the ~~surface of the curved~~ exposed silicon surface region includes producing pores in the exposed silicon surface region, the pores having a diameter of less than 20 nm.

20. (Currently Amended) The method of claim[[s]] 16, wherein thermally oxidizing the ~~at least one~~ roughened silicon surface region forms a silicon dioxide layer having a thickness larger than the depth of the pores.

21. (Currently Amended) A method of producing a storage trench capacitor for a memory cell ~~having~~ including an isolation collar, comprising:

providing a semiconductor substrate, the semiconductor substrate ~~having~~ including a main surface;

providing a trench in the semiconductor substrate, the trench extending from the main surface, the trench ~~having~~ including an upper portion, a lower portion, and a bottom portion, the

upper portion being disposed above the lower portion which is disposed above the bottom portion, and wherein the trench ~~having~~ includes a curved inner surface of silicon;

forming a first electrode of the capacitor in the semiconductor substrate adjacent to the bottom portion of the trench, forming a dielectric layer in the bottom portion of the trench and forming a second electrode of the capacitor in the bottom portion of the trench;

masking the silicon surface region of the upper portion of the trench which is not to be oxidized with a masking layer;

exposing the silicon surface portion in the lower portion of the trench on which ~~the~~ a silicon dioxide layer is to be formed;

roughening the ~~surface of the curved~~ exposed silicon surface region in the lower portion of the trench to produce a layer of porous silicon, the masking layer ~~having~~ including a material which prevents roughening of an underlying material during roughening of the ~~curved surface~~ exposed silicon surface region; and

thermally oxidizing the roughened ~~curved~~ silicon surface region.

22. (Original) The method of claim 21, wherein the masking layer includes silicon nitride.

23. (Currently Amended) The method of claim 21, wherein roughening the surface of the ~~curved~~ exposed silicon surface region includes etching the exposed silicon surface region.

24. (Currently Amended) The method of claim 21, wherein roughening the surface of the ~~curved~~ exposed silicon surface region includes producing pores in the exposed silicon surface region, the pores having a diameter of less than 20 nm.

25. (Currently Amended) The method of claim 21, wherein thermally oxidizing the ~~at least one~~ roughened silicon surface region forms a silicon dioxide layer having a thickness

larger than the depth of the pores.

26. (Original) The method of claim 1, wherein the silicon surface region includes polycrystalline silicon.

27. (New) A method of forming a silicon dioxide layer, comprising:

providing a semiconductor substrate, the semiconductor substrate including at least one silicon surface region with a curved surface;

roughening the surface of the at least one silicon surface region to produce a layer of porous silicon, wherein roughening the surface of the at least one silicon surface region includes etching the surface region in a solution including H_2SO_4, HF and HNO_3 to form pores, the pores each having a width of less than 20 nm and a pore depth of less than 20 nm;

thermally oxidizing the at least one roughened curved silicon surface region; and

oxidizing the at least one silicon surface region to produce an oxidized portion within the semiconductor substrate which ends at a depth, the depth being greater than the pore depth of the pores.

28. (New) A method of forming a silicon dioxide layer, comprising:

providing a semiconductor substrate, the semiconductor substrate including at least one silicon surface region with a curved surface;

roughening the surface of the at least one silicon surface region to produce a layer of porous silicon, wherein roughening the surface of the at least one silicon surface region includes etching the surface region with a mixture of 49% aqueous hydrofluoric acid and pure ethyl alcohol at a ratio of 0.75:0.25 to form pores, the pores each having a width of less than 20 nm and a pore depth of less than 20 nm;

thermally oxidizing the at least one roughened curved silicon surface region; and

oxidizing the at least one silicon surface region to produce an oxidized portion within the

semiconductor substrate which ends at a depth, the depth being greater than the pore depth of the pores.

29. (New) A method of forming a silicon dioxide layer, comprising:

providing a semiconductor substrate, the semiconductor substrate including at least one silicon surface region with a curved surface, wherein the at least one silicon surface region includes monocrystalline silicon;

roughening the surface of the at least one silicon surface region to produce a layer of porous silicon, wherein roughening the surface of the at least one silicon surface region includes forming pores, the pores each having a width of less than 20 nm and a pore depth of less than 20 nm;

thermally oxidizing the at least one roughened curved silicon surface region; and

oxidizing the at least one silicon surface region to produce an oxidized portion within the semiconductor substrate which ends at a depth, the depth being greater than the pore depth of the pores.